

WHAT IS CLAIMED IS:

1. A phase locked loop comprising:
 - 5 a phase-frequency detector that detects a phase difference between a reference signal introduced into a first input terminal and an input signal introduced into second input terminal, and that generates output pulses according to the phase difference;
 - 10 a charge pump that outputs electric current according to an output signal from the phase-frequency detector;
 - a loop filter that attenuates a charge pump output of the charge pump;
 - a voltage controlled oscillator in which the frequency of an oscillator output signal is controlled according to an output voltage of the loop filter;
 - a programmable divider which divides the oscillator output signal from the voltage-controlled oscillator according to input division number data and feeds it back
 - 20 to the second input terminal of the phase-frequency detector,
 - a first modulator that transforms an incoming baseband signal into an integer signal for specifying a division number and that sends the integer signal to a
 - 25 control terminal of the programmable divider;

a second modulator which shapes the incoming baseband signal into a prescribed signal waveform and sends it to the voltage controlled oscillator; and

5 a loop bandwidth selector which changes the loop bandwidth according to a control signal.

2. The phase locked loop according to Claim 1, further comprising:

10 a controller which adjusts a phase error between the first modulator and the second modulator.

3. The phase locked loop according to Claim 1, wherein the loop bandwidth selector changes the loop bandwidth as follows:

15 the loop bandwidth is broadened upon input of a signal to activate the phase locked loop, then convergence to a frequency occurs which depends on a constant representing a carrier frequency, and after a prescribed time, the loop bandwidth is narrowed.

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4. The phase locked loop according to Claim 1, wherein the loop bandwidth selector comprises a variable current charge pump circuit in which the output current value is selected from at least two current value options.

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5. The phase locked loop according to Claim 1, wherein
the first modulator further comprises:

a multiplier which multiplies the baseband signal by a
constant;

5 a sigma delta circuit which carries out sigma delta
modulation of output of the multiplier; and

an adder which adds a constant representing a carrier
frequency to the output of the sigma delta circuit.

10 6. The phase locked loop according to Claim 1, wherein
the first modulator further comprises:

a digital filter which transforms the baseband signal
into a prescribed signal waveform;

15 a sigma delta circuit which carries out sigma delta
modulation of the output of the digital filter; and

an adder which adds a constant representing a carrier
frequency to the output of the sigma delta circuit.

7. The phase locked loop according to Claim 5, wherein
20 the sigma delta circuit is a first order or second order
sigma delta circuit.

8. The phase locked loop according to Claim 5, wherein
the sigma delta circuit comprises a plurality of sigma delta
25 circuits.

9. The phase locked loop according to Claim 1, wherein
the first modulator comprises a multiplier that is
structured to multiply the baseband signal by a constant;

5 a delta modulation circuit that is structured to carry
out delta modulation of the output of the multiplier; and
an adder that is structured to add a constant
representing a carrier frequency to the output of the delta
modulation circuit.

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10. The phase locked loop according to Claim 1,
wherein the first modulator further comprises:
a digital filter which transforms the baseband signal into
a prescribed signal waveform;
15 a delta modulation circuit which carries out delta
modulation of the output of the digital filter; and
an adder which adds a constant representing a carrier
frequency to the output of the delta modulation circuit.

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11. The phase locked loop according to Claim 1,
wherein the second modulator is a pulse shaping circuit
which comprises a digital filter for shaping the baseband
signal into a prescribed signal waveform and a
digital/analog converter.

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12. A data transmission circuit comprising:

- a phase-frequency detector that detects a phase difference between a reference signal introduced into a first input terminal and an input signal introduced into second input terminal, and that generates output pulses according to the phase difference;
- a charge pump that outputs electric current according to an output signal from the phase-frequency detector;
- 10 a loop filter that attenuates a charge pump output of the charge pump;
- a voltage controlled oscillator in which the frequency of an oscillator output signal is controlled according to an output voltage of the loop filter; and
- 15 a programmable divider which divides the oscillator output signal from the voltage-controlled oscillator according to input division number data and feeds it back to the second input terminal of the phase-frequency detector,
- 20 a first modulator that transforms an incoming baseband signal into an integer signal for specifying a division number and that sends the integer signal to a control terminal of the programmable divider;

a second modulator which shapes the incoming baseband signal into a prescribed signal waveform and sends it to the voltage controlled oscillator;

5 a loop bandwidth selector which changes the loop bandwidth according to a control signal;

an amplifier which is connected with the oscillator output of the voltage controlled oscillator in the phase locked loop; and

10 a control circuit structured to provide:
 a loop bandwidth control signal to change the loop bandwidth of the phase locked loop;

 an On/Off signal which turns on or off the amplifier;
and

15 a reference signal and a baseband signal for the phase locked loop,

 wherein the baseband signal incoming is amplified and outputted.

20 13. A method for providing a variable loop bandwidth phase locked loop comprising:

 transforming in a first modulator that has a sigma delta circuit a baseband signal into an integer signal for specifying a division number;

sending the integer signal to a control terminal of
a programmable divider;

shaping in a second modulator an incoming baseband
signal into a prescribed signal waveform and that sends it
5 to a voltage controlled oscillator;

sending an oscillation signal from the voltage
controlled oscillator to the programmable divider;

providing a variable current charge pump which
changes the loop bandwidth of the phase locked loop
10 according to a control signal from a control circuit;

providing a phase-frequency detector for receiving a
reference signal from a controller and the oscillator signal
from the programmable divider; and

inputting at an input a succession of "1" signals,
15 wherein no modulated signal degradation occurs, and wherein
even at a high symbol rate, the reference signal frequency
remains low and sampling frequencies of the phase-frequency
detector and the sigma delta circuit remain low.

20 14. The method for providing a variable loop bandwidth phase
locked loop of claim 13 wherein the first modulator
transforms a baseband signal into an integer signal for
specifying a division number by:

25 multiplying in a multiplier a transmission pulse
train by a constant;

transforming in the sigma delta circuit an output of the multiplier into a prescribed pulse train;

averaging in an averaging circuit an average of outputs from the sigma delta circuit in a given zone;

5 adding in an adder a constant representing a carrier frequency to the output of the averaging circuit; and

outputting a division integer to the programmable divider.

10 15. The method for providing a variable loop bandwidth phase locked loop of claim 13 wherein the first modulator transforms a baseband signal into an integer signal for specifying a division number by:

15 attenuating in a digital filter the baseband signal to a prescribed waveform;

transforming in the sigma delta circuit an output of the multiplier into a prescribed pulse train;

averaging, in an averaging circuit, an average of 20 outputs from the sigma delta circuit in a given zone;

adding in an adder a constant representing a carrier frequency to the output of the averaging circuit; and

outputting a division integer to the programmable divider.

16. The method for providing a variable loop bandwidth phase
5 locked loop of claim 13 wherein the first modulator
transforms a baseband signal into an integer signal for
specifying a division number by:

reading from a data table a transmission waveform
10 which depends on the baseband signal;
introducing the transmission waveform into the sigma
delta circuit;
transforming in a sigma delta circuit an output of the
multiplier into a prescribed pulse train;
15 averaging in an averaging circuit an average of
outputs from the sigma delta circuit in a given zone;
adding in an adder a constant representing a carrier
frequency to the output of the averaging circuit; and
outputting a division integer to the programmable
20 divider.

17. The method for providing a variable loop bandwidth
phase locked loop of claim 13:

wherein the second modulator comprises a pulse shaping circuit.

18. The method for providing a variable loop bandwidth phase
5 locked loop of claim 17 wherein the sigma delta circuit provided comprises a first order sigma delta circuit for:

inputting an input signal $x(n)$ which is output from the multiplier; and

10 outputting the integer signal from a quantizer which outputs an integer closest to a value of the input signal to an adder and to a delay circuit wherein the delay circuit adjusts a phase difference to eliminate phase error between the pulse shaping circuit and the adder.

15 19. The method for providing a variable loop bandwidth phase locked loop of claim 17 wherein the sigma delta circuit provided comprises a second order sigma delta circuit for:

20 inputting an input signal $x(n)$ which is output from the multiplier;

outputting the integer signal from a quantizer which outputs an integer closest to a value of the input signal to an adder and to a delay circuit and a multiplier;

wherein the delay circuit adjusts a phase difference to eliminate phase error between the pulse shaping circuit and the adder;

and wherein a multiplier multiplies the output of the
5 delay circuit by a constant.

20. The method for providing a variable loop bandwidth phase locked loop of claim 17 wherein the sigma delta circuit provided comprises:

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using a plurality of stable sigma delta circuits which are lower than the second order level to make up a second order or higher-level multi-stage sigma delta circuit to assure stable operation.

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